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| APPLICATION NO.                  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|----------------------------------|-------------|----------------------|---------------------|------------------|
| 10/590,955                       | 08/28/2006  | Kazunori Hiramatsu   | 9319S-001754/US/NP  | 4384             |
| 27572                            | 7590        | 06/29/2009           | EXAMINER            |                  |
| HARNESS, DICKEY & PIERCE, P.L.C. |             |                      |                     | SPAR, ILANA L    |
| P.O. BOX 828                     |             | ART UNIT             |                     | PAPER NUMBER     |
| BLOOMFIELD HILLS, MI 48303       |             | 2629                 |                     |                  |
|                                  |             | MAIL DATE            |                     | DELIVERY MODE    |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 10/590,955             | HIRAMATSU, KAZUNORI |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | ILANA SPAR             | 2629                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 28 August 2006.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-6 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 28 February 2006 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date 8/28/2006, 7/7/2008.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent Publication No. 2006/0164405).

With reference to claim 1, Zhou teaches a method for driving an electrophoretic display comprising:

a first reset step of setting a plurality of electrophoretic devices to a second non-display state in which no image is displayed and afterimages caused by writing first image data in a first writing step may be present by applying a first voltage to the plurality of electrophoretic devices between the first writing step for writing the first image data representing a first image in the plurality of electrophoretic devices so as to display the first image on the plurality of electrophoretic devices and a second writing

step for writing second image data representing a second image in the plurality of electrophoretic devices so as to display the second image on the plurality of electrophoretic devices (see paragraphs 40-42, particularly paragraph 40, lines 12-14 and paragraph 42, lines 8-13 and lines 21-24); and

a second reset step for applying a second voltage serving as the non-display-without-afterimage voltage to the plurality of electrophoretic devices so as to set the plurality of electrophoretic devices to the first non-display state at a frequency less than that at which the first reset step is performed (see paragraph 33, lines 3-11).

In the cited embodiment, Zhou fails to teach that the voltage of the first reset step is lower than the voltage of the second reset step.

In the Proposed Solution (see paragraph 44), Zhou teaches that the first voltage is lower than a non-display-without-afterimage voltage for setting the plurality of electrophoretic devices to a first non-display state in which no image is displayed and the afterimages are not present (see paragraph 42, lines 8-13 and paragraph 45, lines 5-10 and lines 14-20).

Specifically, Zhou teaches in the first embodiment (explained under Driving Scheme, see paragraph 39) that during the reset period, the pixels are reset to one of the two extreme levels, either black or white, according to which ever level the pixel is already nearest to, such that the change in gray level is not more than 50%. In this embodiment, Zhou also teaches that the forced reset can be utilized less frequently than the regular reset, and that in the forced reset any afterimages are cleared from the display to improve image quality. In the second embodiment, Zhou teaches using an

over-reset period in which the pixels are driven to an extreme state that is farther from the current state, such that the change in gray level is more than 50%, with the purpose of clearing any afterimages from the display. As would be obvious to one of ordinary skill in the art, a higher voltage is required to make the transition to an extreme level that is farther from the current pixel level than to an extreme level that is closer, such that the regular reset voltage is lower than the forced reset voltage, which is analogous to the over-reset voltage of the second embodiment.

With reference to claim 2, Zhou teaches all that is required with reference to claim 1, and further teaches a determination step of determining whether or not erasing the afterimages is necessary, wherein when it is determined that erasing the afterimages is necessary in the determination step, the second reset step is performed (see paragraph 33, lines 11-15).

Specifically, Zhou teaches that the user can determine that the image quality is unacceptable, thus requiring the erasing of afterimages, and at that time choose to perform the forced reset step.

With reference to claim 3, Zhou teaches all that is required with reference to claim 2, and further teaches that the determination step is performed by perceiving the afterimages or detecting the presence of afterimages (see paragraph 33, lines 11-15).

Specifically, Zhou teaches that the user determines that the image quality drop to an unacceptable level, due to the presence of afterimages, and at that time can choose to perform the forced reset step.

With reference to claim 4, Zhou teaches an electrophoretic display comprising:

a plurality of electrophoretic devices (see paragraph 31, lines 4-6 and paragraph 34, lines 2-4); and

a controlling unit (see paragraph 31, line 4)

for performing a first reset for applying a first voltage to the plurality of electrophoretic devices between the first writing for writing first image data representing a first image in the plurality of electrophoretic devices so as to display the first image, on the plurality of electrophoretic devices and a second writing for writing second image data representing a second image in the plurality of electrophoretic devices so as to display the second image on the plurality of electrophoretic devices (see paragraphs 40-42, particularly paragraph 40, lines 12-14 and paragraph 42, lines 8-13 and lines 21-24) and

for performing a second reset for applying a second voltage serving as the non-display-without-afterimage voltage to the plurality of electrophoretic devices so as to set the plurality of electrophoretic devices to the first non-display state at a frequency less than that at which the first reset is performed (see paragraph 33, lines 3-11).

In the cited embodiment, Zhou fails to teach that the voltage of the first reset step is lower than the voltage of the second reset step.

In the Proposed Solution (see paragraph 44), Zhou teaches that the first voltage is lower than a non-display-without-afterimage voltage for setting the plurality of electrophoretic devices to a first non-display state in which no image is displayed and afterimages caused by the first writing are not present (see paragraph 42, lines 8-13 and paragraph 45, lines 5-10 and lines 14-20).

Specifically, Zhou teaches in the first embodiment (explained under Driving Scheme, see paragraph 39) that during the reset period, the pixels are reset to one of the two extreme levels, either black or white, according to which ever level the pixel is already nearest to, such that the change in gray level is not more than 50%. In this embodiment, Zhou also teaches that the forced reset can be utilized less frequently than the regular reset, and that in the forced reset any afterimages are cleared from the display to improve image quality. In the second embodiment, Zhou teaches using an over-reset period in which the pixels are driven to an extreme state that is farther from the current state, such that the change in gray level is more than 50%, with the purpose of clearing any afterimages from the display. As would be obvious to one of ordinary skill in the art, a higher voltage is required to make the transition to an extreme level that is farther from the current pixel level than to an extreme level that is closer, such that the regular reset voltage is lower than the forced reset voltage, which is analogous to the over-reset voltage of the second embodiment.

With reference to claim 5, Zhou teaches all that is required with reference to claim 4, and further teaches an input unit for inputting a command indicating that erasing the afterimages is necessary, wherein when the command indicating that erasing the afterimages is necessary is input, the control unit performs the second reset (see paragraph 33, lines 11-15 and paragraph 35, lines 22-24).

With reference to claim 6, Zhou teaches a storage display comprising:  
a plurality of memory devices (see paragraph 31, lines 4-6 and paragraph 2, lines 4-5); and

a controlling unit (see paragraph 31, line 4)  
for performing a first reset for applying a first voltage to the plurality of memory devices between the first writing for writing first image data representing a first image in the plurality of memory devices so as to display the first image on the plurality of memory devices and a second writing for writing second image data representing a second image in the plurality of memory devices so as to display the second image on the plurality of memory devices (see paragraphs 40-42, particularly paragraph 40, lines 12-14 and paragraph 42, lines 8-13 and lines 21-24) and

for performing a second reset for applying a second voltage serving as the non-display-without-afterimage voltage to the plurality of memory devices so as to set the plurality of memory devices to the first non-display state at a frequency less than that at which the first reset is performed (see paragraph 33, lines 3-11).

In the cited embodiment, Zhou fails to teach that the voltage of the first reset step is lower than the voltage of the second reset step.

In the Proposed Solution (see paragraph 44), Zhou teaches that the first voltage is lower than a non-display-without-afterimage voltage for setting the plurality of memory devices to a first non-display state in which no image is displayed and afterimages caused by the first writing are not present (see paragraph 42, lines 8-13 and paragraph 45, lines 5-10 and lines 14-20).

Specifically, Zhou teaches in the first embodiment (explained under Driving Scheme, see paragraph 39) that during the reset period, the pixels are reset to one of the two extreme levels, either black or white, according to which ever level the pixel is

already nearest to, such that the change in gray level is not more than 50%. In this embodiment, Zhou also teaches that the forced reset can be utilized less frequently than the regular reset, and that in the forced reset any afterimages are cleared from the display to improve image quality. In the second embodiment, Zhou teaches using an over-reset period in which the pixels are driven to an extreme state that is farther from the current state, such that the change in gray level is more than 50%, with the purpose of clearing any afterimages from the display. As would be obvious to one of ordinary skill in the art, a higher voltage is required to make the transition to an extreme level that is farther from the current pixel level than to an extreme level that is closer, such that the regular reset voltage is lower than the forced reset voltage, which is analogous to the over-reset voltage of the second embodiment.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ILANA SPAR whose telephone number is (571)270-7537. The examiner can normally be reached on Monday-Thursday 8:00-4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571)272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bipin Shalwala/  
Supervisory Patent Examiner, Art Unit 2629

ILS